Abstract of the Disclosure

A shift register device includes transistor pass gates and latches connected in series and disposed along a data bit line, each latch connected to a corresponding transistor pass gate. Each transistor pass gate is controlled by a separate control signal input line that a provides a signal to the transistor pass gate connected to it. The signals are provided in a staggered time pattern beginning with a latch disposed last in succession, shifting data from one position to the next succeeding position. Each latch is capable of storing one bit of data. The shift register utilizes less silicon space while reducing the amount of power consumed during operation.